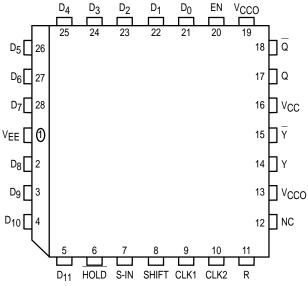
12-Bit Parity Generator/Checker

The MC10E/100E160 is a 12-bit parity generator/checker. The Q output is HIGH when an odd number of inputs are HIGH. A HIGH on the Enable input (EN) forces the Q output LOW.

The E160 also features an output register. Multiplexers direct the register input, giving the option of holding present data by asserting HOLD LOW, or of shifting data in through the S-IN pin by asserting SHIFT HIGH. The output register itself is clocked by a positive edge on CLK1 or CLK2 (or both). A HIGH on the reset pin (R) overrides to force the Y output LOW.

- Provides Odd-HIGH Parity of 12 Inputs
- Shiftable Output Register with Hold
- 900ps Max. D to Q/Q Output
- Enable
- · Asynchronous Register Reset
- Dual Clocks
- Extended 100E VEE Range of 4.2V to 5.46V
- 75kΩ Input Pulldown Resistors

Pinout: 28-Lead PLCC (Top View)



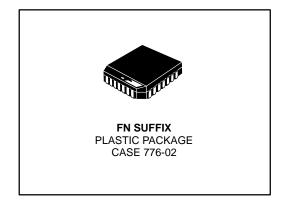
* All V_{CC} and V_{CCO} pins are tied together on the die.

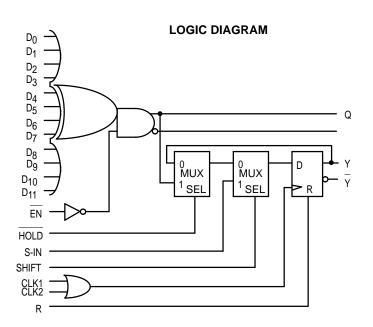
PIN NAMES

Pin	Function					
D ₀ – D ₁₁	Data Inputs					
<u>S-I</u> N	Serial Data Input					
<u>EN</u>	Enable, active LOW					
HOLD	Hold, active LOW					
SHIFT	Shift, active HIGH					
CLK1, CLK2	Clock Inputs					
R _	Reset Inputs					
Q <u>, Q</u>	Direct Output					
Y, Y	Register Output					

MC10E160 MC100E160

12-BIT PARITY GENERATOR/CHECKER





REV 2



12/93

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DC CHARACTERISTICS (VEE = VEE(min) to VEE(max); VCC = VCCO = GND)

		0°C		25°C			85°C					
Symbol	Characteristic	min	typ	max	min	typ	max	min	typ	max	Unit	Condition
lіН	Input HIGH Current										μΑ	
	CLK1, CLK2			200			200			200		
	R	l		300			300			300		
	All Other Inputs			150			150			150		
IEE	Power Supply Current										mA	
	10E		82	98		82	98		82	98		
	100E		82	98		82	98		94	113		

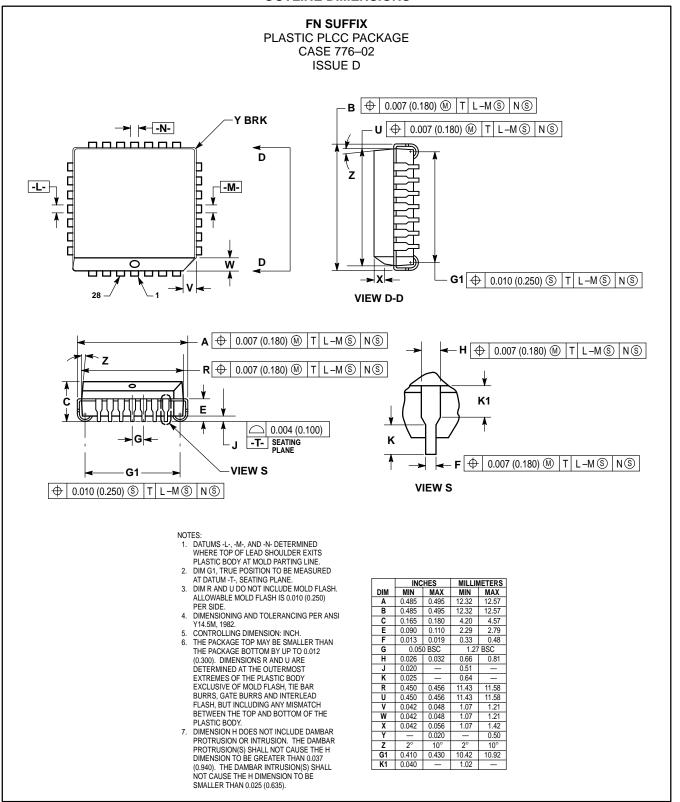
AC CHARACTERISTICS ($V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = V_{CCO} = GND$)

		0°C			25°C			85°C				
Symbol	Characteristic	min	typ	max	min	typ	max	min	typ	max	Unit	Condition
tPLH	Propagation Delay to Output										ps	
tPHL	D to Q	400	650	950	400	650	950	400	650	950		
	En to Q	300	550	750	300	550	750	300	550	750		
	CLK to Y	275	500	700	275	500	700	275	500	700	1	
	R to Y	275	500	725	275	500	725	275	500	725		
t _S	Setup Time										ps	
	<u>D</u>	1200	900		1200	900		1200	900			
	HOLD	600	300		600	300		600	300			
	S-IN	350	150		350	150		350	150			
	SHIFT	500	250		500	250		500	250			
th	Hold Time										ps	
	D	- 400	- 900		- 400	- 900		- 400	- 900			
	HOLD	100	- 300		100	- 300		100	- 300			
	S-IN	300	-150		300	-150		300	-150			
	SHIFT	200	- 250		200	- 250		200	- 250			
t _r	Rise/Fall Time			·					_		ps	
tf	20 - 80%	300	450	650	300	450	650	300	450	650		

Within a device skew is guaranteed for identical transitions on similar paths through a device.

MOTOROLA 2–2

OUTLINE DIMENSIONS



MC10E160 MC100E160

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